IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of

Andreas Schrader and Darren Carlson — Confirmation No. 3819

Serial No. 10/603,749 — Group Art Unit 2616

Filed June 26, 2003 — Examiner Ian N. Moore

For MECHANISM FOR TRANSMISSION OF TIME-SYNCHRONOUS DATA

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

APPELLANT'S BRIEF UNDER 37 C.F.R. §41.37

This brief is in furtherance of the Notice of Appeal, filed in this case on January 23, 2009.

This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. §41.37(c)):

I. REAL PARTY IN INTEREST

II. RELATED APPEALS AND INTERFERENCES

III. STATUS OF CLAIMS

IV. STATUS OF AMENDMENTS

V. SUMMARY OF CLAIMED SUBJECT MATTER

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

VII. ARGUMENTS

☐ ARGUMENT VIIA. REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

I. REAL PARTY IN INTEREST

The real party in interest in the appeal is:

☐ the party named in the caption of this brief.

☑ the following party: NEC Corporation of Tokyo, Japan

II. RELATED APPEALS AND INTERFERENCES

With respect to other appeals, interferences or judicial proceedings that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal:

☑ there are no related appeals, interferences or judicial proceedings related to, which directly affect or may be directly affected by or have a bearing on the Board's decision in this pending Appeal.

☐ these are as follows:

III. Status of Claims

The status of the claims in this application are:

A. Total number of claims in Application

Claims in the application are: Claims 1 to 18

B. Status of all the claims:

1. Claims cancelled: None
2. Claims withdrawn from consideration but not cancelled: None
3. Claims pending: Claims 1 to 18
4. Claims allowed: None
5. Claims rejected: Claims 1 to 18

C. Claims on Appeal.

The claims on appeal are: Claims 1 to 18

IV. Status of Amendments

The status of amendments filed subsequent to the final rejection are as follows: An amendment under 37 C.F.R. 1.116 was filed on December 29, 2008, for the purpose of making minor corrections to the claims in response to the Examiner's Claim Objections set out on pages 8 and 9 of the Office Action mailed September 30, 2008. In the Office Action mailed January 22, 2009, the Examiner stated that the amendment would be entered upon appeal. The claims presented in the Claims Appendix are as amended by the amendment filed December 29, 1998.

V. Summary of Claimed Subject Matter

The invention as defined in the claims on appeal is directed to a mechanism for the transmission of time-synchronous mulitmedia data from sender to receiver using a network, especially the Internet, where the data is processed and/or transmitted with at least one processing unit at the sender and/or the receiver. A processing unit can contain several subcomponents for filtering, processing, compressing, packetizing of data, buffering, etc. The mechanism according to the claimed invention improves the transmission quality for time-synchronous multimedia data by setting up and adapting a parallel processing unit based on changed data load and/or network characteristics. After a switching process, preferably using a switch, the data is processed and/or transmitted using the parallel processing unit.

Mechanisms for the transmission of time-synchronous data are well-known in practice and are very well suited for the transmission of multimedia purposes, like video conferences, telephone calls and others. This is especially true in the context of transmitting data over Internet Protocol (IP) networks. The most common networks are usually only configured for the transmission of scalable, time-insensitive applications, like e.g. Internet-Browsing. Due to their intrinsic structure, these networks are not well suited for the transmission of time-synchronous data. To improve the transmission quality, mechanisms have been developed, which allow for the transmission of time-synchronous data, especially multimedia data, in real-time. The goal of these mechanisms is to improve the QoS - Quality of Service - by treating time-synchronous data with a higher priority for transmission than other traffic. The transmission of time-synchronous data, which are most often transmitted in a compressed format, is especially difficult, since the data must be available at the receiver at a precise time in order to allow for timely proper decoding and rendering.

To best understand the disclosed and claimed invention, it is necessary to understand the most relevant prior art which is illustrated in Figure 1 and shows an

embodiment of a known mechanism for the transmission of time-synchronous data from a sender 1' to a receiver 2' over a network. The data is processed and transmitted at the sender side using the processing unit 3'. The network characteristics are changing and, therefore, the processing unit 3' is not any more suited to process the data, e.g., to compress and to divide the data into packets, such that a sufficient transmission quality can be achieved at the receiver. In this example, the data represent raw video frames at a frame rate f [1/s]. Figure 2 shows the respective time order of the mechanism of Figure 1. Sender 1' produces data as unprocessed synchronized video frames with frame rate f [1/s]. The raw frames are passed to the processing unit 3' and have length $\Delta t = 1/f$. The frames are therefore passed to the processing unit 3' at synchronous times $\{t_0, t_0+\Delta t, t_0+2\Delta t, \ldots\}$. The time, necessary to construct processing unit 3' with a codec 6a', a filter 6b', and a packetizer 6c' as well as all other required resources is denoted as $\sigma 1$. At time t_0 the processing unit 3' is ready for transmission and the first frame 1 will be processed and transmitted. The intrinsic delay of processing unit 3' is denoted as δ_1. This denotes the time required inside processing unit 3' to process 1 frame and to produce data output. Intrinsic delay can be observed for example in modern video codecs, which mode of inter-frame processing is based on the so-called GOP - Group of Picture. A GOP consists of different image types, where B-frames - bi-directional frames - are only processed and played, if a previous or following I-frame - intra-coded frame - is available in the internal buffer. Typical GOPs like for example in the MPEG format, consist of nine frames, e.g., IBBPBBPBB. The output of data through the processing unit 3' is therefore only possible at times $\{t_0+\delta_1, t_0+\delta_1+\Delta t, t_0+\delta_1+2\Delta t, \ldots\}$.

The time necessary to release all required resources of processing unit 3' is denoted as ϕ_i. The releasing process is therefore finished at time $t_0+\delta_1+i\Delta t+\phi_i$. Now, a new processing unit 3" (not shown) is assembled, which requires σ_2 seconds. Under the assumption that the data processing within processing unit 3" can not be assembled faster than real-time, this leads to the fact, that the processing of frames

can only be started after the input of a complete frame. Therefore, the next frame after finishing the assembly process of the new processing unit 3" is frame number j. The time until frame j is completely available is denoted as resync gap. The processing unit 3" starts the processing of the input data at time t_0' and the transmission of the first processed at time $t_0'+\delta_2$ due to the intrinsic delay σ_2. This means, that during the time period $t_\gamma = [t_0 + \delta_1 + i\Delta t, t_0' + \sigma_2]$ no data output can be generated. This time period is donated as gap time t_γ.

The time when the new processing unit 3" is starting up can be computed as

$$
\begin{aligned}
t_0' &= t_0 + \left\lceil \frac{\delta_1 + i\Delta t + \phi_1 + \sigma_2}{\Delta t} \right\rceil \Delta t \\
&= t_0 + \left\lceil \frac{\delta_1 + i\Delta t + \phi_1 + \sigma_2}{\Delta t} \right\rceil \Delta t
\end{aligned}
$$

For the loss time t_λ, the following is true:

$$
\begin{aligned}
t_\lambda &= (j-1)\Delta t - \Delta t \\
&= \left\lceil \frac{\delta_1 + \phi_1 + \sigma_2}{\Delta t} \right\rceil
\end{aligned}
$$

With this, the number λ of unprocessed frames during this time period can be computed as

$$
\begin{aligned}
\lambda &= j - 1 - i \\
&= \left\lceil \frac{\delta_1 + \phi_1 + \sigma_2}{\Delta t} \right\rceil
\end{aligned}
$$

The gap time t_λ is the time, where no data is produced at the output during the adaptation:

$$
\begin{aligned}
t_\lambda &= t_0' + \delta_2 - (t_0 + \delta_1 + i\Delta t) \\
&= t_0 + \left\lceil i \frac{\delta_1 + \phi_1 + \sigma_2}{\Delta t} \right\rceil \Delta t + \delta_2 - t_0 - \delta_1 - i\Delta t \\
&= \left\lceil \frac{\delta_1 + \phi_1 \sigma_2}{\Delta t} \right\rceil \Delta t + (\delta_2 - \delta_1)
\end{aligned}
$$

In the known mechanism shown in Figure 1, t_α is the time needed to fulfill the requested adaptation. It is exactly equivalent to the gap time t_λ: $t_\alpha = t_\lambda$. Problems arise when there are changed data load and/or network characteristics which can result in IP packets getting lost, leading to a significant degradation of media quality. This is especially true in wireless networks due to the intrinsic physical limitations of such networks.

Applicants achieve seamless handovers between potentially many different (arbitrary complex) processing units as a mechanism for optimizing transmission quality in packet-based networks and low-power devices (e.g.., mobile telephones). The central idea is to allow adaption between various independent instantiations of processing units, as determined by a particular operating environment. Processing units may contain arbitrary complex subcomponents (codecs, filters, packetizers, etc.) and may be available locally within a device or downloaded by standard means over a network connection. Applicants claimed invention is novel in that it supports seamless adaption between the current operating processing chain and newly instantiated chains either by feeding data simultaneously to both chains or utilizing additional processing resources for encoding within the second chain during setup.

In the claimed invention, Applicants switch the input of two or more independent processing units, where it is always guaranteed that only one of them is processing at any given time. In addition, Applicants coordinate the control sequence of parallel processing unit operations (setup, teardown or resource sharing) in order to

minimize processing power requirements and allow the installation of potentially useful processing units specific to a given operational environment.

The features which characterize the claimed invention include the following:

- A digital media processing system with arbitrary number of "processing units".
- Generally applicable to real-time IP streaming media scenarios.
- Processing units are "not specified" and may include arbitrary chains of codecs, packetizers, etc.
- Seamless switching is intended to accommodate additional processing units (e.g., downloaded).
- Processing chain components may contain quality settings (e.g., quantizer settings).
- Processing chains are instantiated into memory "on-demand" by adaptation algorithms.
- Seamless switching refers to instantiating a processing unit and activating its input.
- Seamless switching does accommodate processing chain instantiation timing.
- Processing chains are never fed data simultaneously.
- Processing chains never operate on input data simultaneously.
- Seamless switching may include teardown or timed caching of unneeded processing units.

Figure 3 shows a schematic presentation of an embodiment of the mechanism according to the invention for the transmission of time-synchronous data from a sender 1 to a receiver 2 over a network. The data is processed and transmitted at the sender side using the processing unit 3. In the example described, the network characteristics are changing and, therefore, the processing unit 3 is not any more suited to process the data, e.g., to compress and to divide the data into packets, that a sufficient transmission quality can be achieved at the receiver. In this example, the

data represent raw video frames at a frame rate f[1/s].

According to the invention a new processing unit 4 is setup, which is adapted to the new conditions. The schematic drawing in Figure 3 shows the embodiment before switching using the switch 5, such that the processing and transmission of data at that time is performed within processing unit 3. In the embodiment of Figure 3, the data is processed using various subcomponents 6a, 6b, 6c within processing unit 3. In particular, these subcomponents are a codec 6a for the compression of data, a filter 6b for the eventually removing of frames, as well as a packetizer 6c for dividing the data into packets for streaming (e.g., via RTP). In an analogous way, the data is processed in processing unit 4 using various subcomponents 7a, 7b, 7c. Also here, the subcomponents 7a, 7b, and 7c are a codec 7a, a filter 7b, and a packetizer 7c. Within processing unit 3 as well as within the parallel processing unit 4, additional not shown subcomponents for further processing and transmission of frames are foreseen. The data from sender 1 in this example is acquired using a mechanism for capturing visual data, a video camera, and will be forwarded to the processing unit 3, as well as to processing unit 4 after their creation, using an additional switch 8.

Figure 4 shows the time schedule of the mechanism according to the invention under the same pre-conditions as in the prior art embodiment of Figure 2. Equivalent times and data are denoted with the same notations. After time t_0, again a trigger event is generated within the data management system. The time to generate the parallel processing unit is again denoted as time σ_2. Whereas the processing unit 4 is created within the time σ_2, processing unit 3 is processing and transmitting frames, in particular frames up to frame number $j-1$. Afterwards, the switching is performed using the switch 5, such that the parallel processing unit 4 is processing frame number j and no frames get lost. The time, when the parallel processing unit 4 is ready to transmit frames, can be therefore be computed as t_0:

$$
\begin{aligned}
t_0' &= t_0 + \left\lceil \frac{\delta_1 + i\Delta t + \sigma_2}{\Delta t} \right\rceil \Delta t \\
&= t_0 + \left\lceil i + \frac{\delta_1 + \sigma_2}{\Delta t} \right\rceil \Delta t
\end{aligned}
$$

Under the assumption that $t_0' = t_0 + (j - 1)\,\Delta t$, the first output is

$$
j = i + \left\lceil \frac{\delta_1 + \sigma_2}{\Delta t} \right\rceil + 1
$$

and the gap time t_λ can be determined as follows:

$$
\begin{aligned}
t_\lambda &= t_0' + \delta_2 - (t_0 + \delta_1 + (j-1)\Delta t) \\
&= t_0 + (j-1)\Delta t + \delta_2 - (t_0 + \delta_1 + (j-1)\Delta t) \\
&= (\delta_2 - \delta_1)
\end{aligned}
$$

If δ_2 is greater than δ_1, a transmission break will occur, which can be compensated by using a memory buffer. Such memory buffers are already in use for the compensation of jitter and therefore no additional resources are required. The transmission break is actually only caused by the difference of the intrinsic delays of the involved codecs and is not created by the mechanism according to the invention. In any case, the delay is significantly smaller than in the known sequential mechanisms. If δ_2 is less than δ_1, the parallel processing unit is able to transmit the frame j even before the processing unit 3 can process and transmit this frame. In this example, the decision whether processing unit 3 or the parallel processing unit 4 should be used to process and transmit the data is based on the current data rate. The switching process to the parallel processing unit 4 is performed when the data output of the parallel processing unit 4 is smaller than the data output of the processing rate 3. In both cases, no frames will be dropped and therefore the following is true: $t_\lambda = 0$, $\lambda = 0$.

With the mechanism according to the invention it is also true that the overall

adaptation time t_α is smaller, since the parallel processing unit 4 can process and transmit data much earlier:

$$\begin{aligned} t_\alpha &= t_0' + \delta_2 - (t_0 + \delta_1 + i\Delta t) \\ &= t_0 + \left\lceil i + \frac{\delta_1 + \sigma_2}{\Delta t} \right\rceil \Delta t + \delta_2 - t_0 - \delta_1 - i\Delta t \\ &= \left\lceil \frac{\delta_1 + \sigma_2}{\Delta t} \right\rceil \Delta t + (\delta_2 - \delta_1) \end{aligned}$$

The Tables 1 to 4 on pages 15 to 18 show the improvement realized by the invention over the prior art of Figures 1 and 2. In the second case shown in Table 1, a particularly fast setup and adaptation time is assumed, where the codecs exhibit a small delay value and the teardown of the processing unit 3' requires time. The mechanism of the prior art shown in Figure 1 drops seven (7) frames, leading to a gap time t_λ = 330ms. In contrast, the mechanism according to the invention drops no frames. Moreover, the adaptation time is significantly reduced to 130ms, which is an improvement of 61%. The third case assumes that the processing unit 3 can be de-attached immediately, which is an unrealistic assumption. Even so, the mechanism according to the invention still prevents the dripping of seven (7) frames and the gap time t_λ is reduced from 330ms to 50ms. In the last case, codecs with very small intrinsic delay of approximately 10ms are assumed, which is normal for audio codecs. In this case, the prior art mechanism of Figure 1 drops eleven (11) frames and the mechanism of the present invention drops none. the gap time t_λ is reduced from 440ms to zero (0ms). Moreover, the adaptation time t_α using the mechanism according to the invention is almost halved. Tables 2, 3, and 4 list several different combinations for δ = 50ms, 100ms, 200ms, σ = 50ms, 100ms, 500ms, 1,000ms and f = 10ms, 200ms, 400ms. With these tables, the advantages of the mechanism according to the invention are again shown clearly. It should be noted that in

"Seamless Mode", that is, the operation of the claimed invention, listed in the table, no frames are ever lost.

The following tables provide an indication of the support in the specification and drawings for each of the several limitations recited in the claims:

Claim 1	Support
An apparatus for the transmission of time-synchronous multi-media data from a sender to a receiver using a IP (Internet Protocol) network, wherein the time-synchronous data is processed and transmitted at the sender as well as the receiver, comprising:	In Fig. 3, the sender is shown at 1, the receive is shown at 2, and the IP network is indicated by the elongated "S" symbol immediately to the left of receiver 2.
the sender receiving time-synchronous multi-media data;	The data transmitted by the sender 1 is time-synchronous multi-media data as indicated by the symbols at sender 1.
a mechanism connected to said sender for processing the time-synchronous multi-media data for output to said IP network; and	The data is processed by processing units 3 and 4 and output to the IP network via switch 5.
the receiver connected to said IP network for receiving processed time-synchronous multi-media data transmitted over said IP network;	The receiver 2 is connected to the IP network for receiving the processed time-synchronous data transmitted over the IP network.
said mechanism comprising:	

Claim 1	Support
a first processing unit composed of multiple subcomponents, each subcomponent being designed to process the time-synchronous multi-media data in a specific and different way, a plurality of said multiple subcomponents of said first precessing unit being selected from the group consisting of a codec, a filter and an IP packetizer;	The first processing unit 3 is composed of multiple subcomponents, each of which is designed to process the time-synchronous multi-media data in a specific and different way. The subcomponents of the first processing unit 3 include a codec 6a, a filter 6b, and an IP packetizer 6c.

Claim 1	Support
a second processing unit parallel to the first processing unit, said second processing unit being composed of multiple subcomponents, each subcomponent being designed to process the time-synchronous multimedia data in a specific and different way, a plurality of said multiple subcomponents of said second processing unit being selected from the group consisting of a codec, a filter and an IP packetizer, wherein the subcomponents of the second processing unit are setup and adapted based on changed sender data rate or network characteristics by configuring attribute parameters of the subcomponents, wherein data processing and transmission of the time-synchronous multi-media data is continued within the first processing unit during the setup and adaptation of the second processing unit; and	The second processing unit 4 is parallel to the first processing unit 3 and is composed of multiple subcomponents, each of which is designed to process time-synchronous multimedia data in a specific and different way. The subcomponents of the second processing unit 4 include a codec 7a, a filter 7b, and a packetizer 7c. The subcomponents of the second processing unit 4 are setup and adapted based on changed sender data rate or network characteristics by configuring attribute parameters of the subcomponents. The data processing and transmission of the time-synchronous multi-media data is continued within the first processing unit during the setup and adaptation of the second processing unit.

Claim 1	Support
a switch selecting between the first and second processing units, the processing and transmission of the time-synchronous multi-media data initially being performed by the first processing unit and, after switching by the switch, the processing and transmission of the time-synchronous multi-media data is performed using the second processing unit such that the processing and transmission of the time-synchronous multi-media data is performed within the second processing unit, the output of said switch being connected to said IP network.	The switch 5 selected between the first processing unit 3 and the second processing unit 4. The processing and transmission of the time-synchronous multi-media data is initially performed by the first processing unit 3 and, after switching by the switch 5, the processing and transmission of the time-synchronous multi-media data is performed using the second processing unit 4 such that the processing and transmission of the time-synchronous multi-media data is performed within the second processing unit. The output of said switch being connected to said IP network.

Claim 2	Support
The apparatus according to claim 1, wherein the setup and adaptation of the second processing is started using a trigger event.	Specification, page 7, lines 29–31.

Claim 3	Support
The apparatus according to claim 1, wherein the switching is performed after completion of the setup and adaptation of the second processing unit.	Specification, page 8, lines 3–5.

Claim 4	Support
The apparatus according to claim 1, wherein the switching is performed after reaching a certain switching condition.	Specification, page 8, lines 9–12.

Claim 5	Support
The apparatus according to claim 4, wherein the certain switching condition is whether at least one given parameter reaches at a predetermined value.	Specification, page 8, lines 12–15.

Claim 6	Support
The apparatus according to claim 1, wherein the time-synchronous multi-media data is processed in the first processing unit using a plurality of said multiple subcomponents.	Specification, page 12, lines 13–15. In Fig. 3, the first processing unit 3 processes the time-synchronous multi-media data using subcomponents 6a, 6b, 6c, etc.

Claim 7	Support
The apparatus according to claim 6, wherein the subcomponents include at least one of a codec, a filter, a packetizer, and a memory buffer.	Specification, page 8, lines 23–27. Fig. 3 shows the codec 6a, filter 6b, and packetizer 6c. The unlabeled block would be a memory buffer.

Claim 8	Support
The apparatus according to claim 1, wherein the time-synchronous multi-media data is processed in the second processing unit using a plurality of said multiple subcomponents.	Specification, page 8, lines 30–35. Fig. 3 shows the second processing unit 4 which processes the time-synchronous multi-media data using a plurality of said multiple subcomponents.

Claim 9	Support
The apparatus according to claim 8, wherein the subcomponents include at least one of a codec, a filter, a packetizer, and a memory buffer.	Specification, page 8, lines 30–35, page 12, lines 19–23. Fig. 3 shows the subcomponents of the second processing unit 4 to be a codec 7a, a codec 7b, a filter 7c, plus additional subcomponents.

Clam 10	Support
The apparatus according to claim 8, wherein the subcomponents are connected during setup.	Specification, page 12, lines 7–8.

Claim 11	Support
The apparatus according to claim 1, wherein the first and second processing unit is initialized after setup.	Specification, page 9, lines 6–8.

Claim 12	Support
The apparatus according to claim 8, wherein each of the subcomponents of the second processing unit is adapted to the other subcomponents or changed sender data rate or changed network characteristics.	Specification, page 6, lines 14–17.

Claim 13	Support
The apparatus according to claim 6, wherein, after switching by the switch, the subcomponents of the first processing unit are de-attached from each other.	Specification, page 9, lines 29–31.

Claim 14	Support
The apparatus according to claim 13, wherein a plurality of the second processing units is setup and, after switching by the switch, the subcomponents of the first processing unit are included in one of the second processing units.	Specification, page 9, lines 31–33.

Claim 15	Support
The apparatus according to claim 6, wherein after switching by the switch, the subcomponents of the first processing unit remain connected.	Specification, page 9, lines 34–35.

Claim 16	Support
The apparatus according to claim 1, wherein a plurality of second processing units are setup and adapted based on changed data rate and network characteristics.	Specification, page 6, lines 14–17.

Claim 17	Support
The apparatus according to claim 1, wherein an additional processing unit for the processing and transmission of time-synchronous multi-media data is used in sequence with the first and second processing units.	Specification, page 10, lines 11–13.

Claim 18	Support
The apparatus according to claim 1, wherein the time-synchronous multi-media data is gathered with one of mechanisms for acquiring visual data and speech data.	Specification, page 10, lines 34–36, page 12, lines 28–32.

VI. Grounds of Rejection to be Reviewed on Appeal

Claims 1 to 4 and 6 to 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over International Patent Publication WO 00/62254 of Zahn in view of U.S. Patent No. 6,694,373 to Sastry et al.

Claim 5 stands rejected under 35 U.S.C. §103(a) as being unpatentable over International Patent Publication WO 00/62254 of Zahn in view of U.S. Patent No. 6,694,373 to Sastry et al. and U.S. 7,095,717 to Muniere.

Claims 1 to 13, 15, and 18 additionally stand rejected as being unpatentable over U.S. Patent No. 5,299,003 to Ochi in view of U.S. Patent No. 6,694,373 to Sastry et al.

ARGUMENT VIIA. REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

There are no rejections under 35 U.S.C. §112, first paragraph.

ARGUMENT VIIB. REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH

There are no rejections under 35 U.S.C. §112, second paragraph. With the entry of the Amendment Under 37 C.F.R. §1.116, the objections set out on pages 8 and 9 of the Office Action mailed September 30, 2008, are believed to have been overcome.

ARGUMENT VIIC. REJECTIONS UNDER 35 U.S.C. §102

There are no rejections under 35 U.S.C. §102.

ARGUMENT VIID. REJECTIONS UNDER 35 U.S.C. §103

First Rejection Under 35 U.S.C. §103

The first rejection under 35 U.S.C. §103 is that claims 1 to 4 and 6 to 18 are unpatentable over the International Patent Publication WO 00/62254 of Zahn in view of U.S. Patent No. 6,694,373 to Sastry et al.

The primary reference to Zahn is not relevant to the claimed invention. On page 9 of Zahn, the apparatus 1 is described as being connected by a PCI bus 2 to a CPU of a personal computer. "PCI" stands for Peripheral Component Interconnect, a bus standard designed by Intel for personal computers. See page 537, second definition, of *Newton's Telecom Dictionary*, 14^{th} Ed. (1998), copy attached. In other words, the apparatus 1 is a processor board which is inserted into a PCI bus card slot <u>inside</u> a personal computer. Zahn describes Figure 3 as illustrating "temporally sequential data packets like those occurring in video processing". This is <u>not</u> the same thing as time-synchronous data. As described at the top of page 11 of Zahn, "video signal 50 has temporally discrete and sequential data packets, so-called frames 100. . . which have the constant temporal spacing T, . . ." Zahn goes on to describe that a first frame 101 is requested by the dispatcher program of the primary processor along the PCI bus 2 along the local bus 7 of the apparatus 1. This data packet 101 is then decompressed by the decoder 3. This data is clearly <u>not</u> time-synchronous. The data packets are temporarily sequential; that is, they follow one another in a sequential order, but they are static (i.e., stored on hard disk) until requested by the dispatcher program. The last paragraph of page 9 of Zahn describes the internal components of the PCI card apparatus 1. The acronyms "MPEG" and "HDTV" respectively stand for Motion Picture Experts Group and High Definition Television (see pages 341 and 465, *Newton's Telecom Dictionary* by Harry Newton (1998), copies attached). MPEG is a video encoding scheme, and HDTV merely describes a type of television having a 16-to-9 aspect ratio and a prescribed pixel resolution. Non-linear video editors of the type Zahn describes implement MPEG video encoding on video frames that have

resolutions meeting the HDTV definition.

Thus, contrary to the Examiner's contention, Zahn does not disclose transmission of time-synchronous data and certainly does not disclose transmission of that data using a network. On the contrary, Zahn discloses a video processor board for a personal computer (PC) for connection to the Peripheral Component Interconnect (PCI) bus. This video processor board is for non-linear video editing (NLE, see page 4, line 8, of Zahn) systems which, by their very nature, are not transmitting time-synchronous data from a sender to a receiver. The Zahn video processor board may include multiple processors, but their operation is entirely different from the claimed first and second processors. In the case of the Zahn video processor board, the multiple processors are for the purpose of improving rendering speed of the video data being edited. This process is not real time. In contrast, the first and second processing units of the claimed invention operate in a manner to avoid time delays and resulting dropping of frames in the transmission of the time-synchronous data. This is process is real time.

For further explanation of HDTV, NLE systems and video processing expansion cards, see the following attached articles from Wikipedia:

- High-definition television
- Non-linear editing system
- Video processing expansion card

At the heart of any NLE system is a video capture card which is inserted into an option card slot (currently a PCI or PCI express slot) in a PC. Attached is a copy of a paper entitled "Video 101" from ATI corporation, now merged with AMD corporation, which describes the fundamentals. Also attached is a copy of a product brochure for the Matrox RT.X2 system for professional NLE systems which includes a card, similar to the Zahn card, that is inserted into an option card slot of a PC. Home NLE systems are also commonly available, as indicated by the attached pages describing the Turtle Beach Video Advantage PCI video production system. The point

here is that the claimed invention is not a NLE system of the Zahn type.

The declaration under 35 C.F.R. §1.132 of Koichi Funaya, an expert in the art of the disclosed and claimed invention, was submitted with the Amendment Under 37 C.F.R. §1.114 filed February 1, 2008. Mr. Funaya addressed the rejection of claims 13 and 14 under 35 U.S.C. §112, first paragraph, raised by the Examiner and now withdrawn. First of all, in numbered paragraph 3 at the bottom of page 2 of his declaration, Mr. Funaya specifies the level of education and skill in the art one of ordinary skill in the art would have for the disclosed and claimed invention, a person of this level of skill being the criteria for disclosure required under Section 112, first paragraph, and, in addition, for determining obviousness under Section 103. Mr. Funaya also addressed the Zahn reference in numbered paragraph 5 bridging pages 3 and 4 of his declaration under 37 C.F.R. §1.132. Mr. Funaya notes that "Zahn is directed to non-linear video editing which, by definition, is not time-synchronous transmission over a network."

The patent to Sastry et al. discloses a voice processing allocation scheme in an IP network to which multiple clients are connected via servers, as generally shown in Figure 2. The servers have processing modules 430 having multiple Digital Signal Processors (DSPs) 431 to 439. These DSPs implement various algorithms, such as Adaptive Differential Pulse Code Modulation (ADPCM) and Conjugated Structure Algebraic Code-Excited Linear Prediction (CS-ACELP) voice compression. These are processor intensive algorithms, and the problem addressed by Sastry et al. is the switching of active data connections from one processor to another processor without significantly interfering with the transmission of voice and other data. Sastry et al. do this using a DSP resource allocation algorithm to load share the data by selectively moving an active voice call currently being processed by one DSP to another DSP having sufficiently available processing power, without interrupting the prevailing service. The liberated DSP may then be used to process a new voice call. Figure 8 illustrates the data switching between DSPs. By load sharing among the DSPs, the

number of simultaneous active voice calls supported by a voice processing module may be increased.

The DSP load sharing scheme of Sastry et al. is not the same or analogous to the claimed invention. In the claimed invention, adaptation to changed data rate and/or network characteristics has to be performed without further degradations of transmission quality. This is achieved through the setup of a parallel processing unit which is adapted to the changed data rate and/or network characteristics. This is not load sharing among a plurality of identical processors, as in Sastry et al. Rather, what the claimed invention does is to setup a parallel processor in which the individual subcomponents of the parallel processor are adapted to the changed data rate and/or network conditions. Once the parallel processor is setup, that is, the subcomponents of the parallel processor are instantiated and initialized, processing and transmission of the time-synchronous data is performed by switching over to that processor by means of a switch. In this way, the transmission of time-synchronous data from the sender to the receiver over an IP network is carried out without loss of packetized frames so that there is no degradation in the reception of multi-media data at the receiver.

Mr. Funaya also discussed the rejection of claims 1 to 4 and 6 to 18 as being obvious in view of the Zahn and Sastry et al. references in numbered paragraph 7 beginning on page 4 and continuing to the top of page 6 of his declaration under 37 C.F.R. §1.132. Mr. Funaya noted again that claim 1 refers to a mechanism for the transmission of time-synchronous data, but Zahn does not transmit any data but operates on a single machine. As to claim 2, Mr. Funaya notes that this claim refers to the special case of necessity to change the parameters of the system during the transmission but that Zahn does not change the parameters the parameters of a video editing unit after setup. As to claim 3, Mr. Funaya noted that this claim refers to the idea of creating a connection to the second processing unit is only done when the setup and/or adaptation is already realized but that Zahn switches before setup since

the timing problems of component setup time do not matter for video editing. Mr. Funaya notes that claims 6 to 18 refer to different variants of the core concept. Referring to the Sastry et al. patent, Mr. Funaya stated "that in Sastry et al. all the processors are always active and perform processing operation in parallel" whereas "Applicants, on the other hand, disclose and claim a method whereby the second processing unit (or several units) is setup AFTER the switch command (which can't be known in advance in real time traffic and will be based on varying load conditions in the network or the clients)." Mr. Funaya went on to say that "The claimed invention method ensures the DYNAMIC creation and deletion of processing chains, still no loss or interruption in the transmission will appear", whereas "Sastry et al. do not cover the problem of setup time at all."

Not only are Zahn and Sastry et al. not relevant to the disclosed and claimed invention, the combination of Zahn and Sastry would not result in a workable system, much less the Applicants' invention. On the one hand, Zahn is directed to a non-linear video editor operational in a single personal computer, and on the other hand, Sastry et al. discloses a voice processing allocation scheme in an IP network to which multiple clients are connected via servers. Neither are related to the other, and it is unclear how load sharing among multiple identical DSPs which support a number of simultaneous active voice calls can be used in a non-linear video editing mechanism.

Second Rejection Under 35 U.S.C. §103

The second rejection under 35 U.S.C. §103(a) is that claim 5 is unpatentable over International Patent Publication WO 00/62254 of Zahn in view of U.S. Patent No. 6,694,373 to Sastry and U.S. 7,095,717 to Muniere.

As discussed above, Zahn does not disclose the basic system recited in claim 1. The Zahn video processor board is for an entirely different function and is constructed and operates in a manner which is entirely different from the disclosed and claimed invention. The Sastry et al. load sharing scheme is not the same as the

claimed setup of a parallel processor with subcomponents adapted for the changed data rate or network conditions. Muniere discloses a method for multiplexing two data flows on a radio communication channel and corresponding transmitter. Since Zahn is not transmitting data from a sender to a receiver, Muniere cannot be combined with Zahn to make a workable system. The two are in entirely different technical fields. Moreover, the claimed invention has nothing whatsoever to do with multiplexing two data flows. On the contrary, the claimed invention is concerned with the transmission of one data flow only, the time-synchronous multi-media data. Clearly there is no basis in fact for the conclusion of obviousness based on Zahn in combination with Sastry et al. and Muniere.

Mr. Funaya addressed the rejection of claim 5 in numbered paragraphs 8 and 9 on page 6 of his declaration under 37 C.F.R. §1.132. Mr. Funaya first of all notes that "Muniere proposes a multiplexing method to ensure prioritized transmission of high priority data with enough remaining bandwidth for the low priority data to flow." Mr. Funaya notes that "In real time transmission of multimedia data of packet networks, the transmission quality of the channel can vary quickly and significantly over time." Mr. Funaya states that "claim 5 specifies a solid method for the identification of an appropriate switching condition" and Muniere does not specify any conditions, since there is no switch involved in the Muniere multiplexing method. Moreover, neither Zahn nor Sastry et al. refer to the same decision as given in claim 5.

Third Rejection Under 35 U.S.C. §103

The third rejection under 35 U.S.C. §103 is that claims 1 to 13, 15, and 18 are unpatentable over U.S. Patent No. 5,299,003 to Ochi et al. in view of U.S. Patent No. 6,694,373 to Sastry.

Ochi et al. do <u>not</u> disclose an apparatus for the transmission of time-synchronous multi-media data from a sender to a receiver using a IP (Internet

Protocol) network; rather, what Ochi et al. disclose is a signal processing apparatus for a magnetic video tape recorder. The Ochi et al. signal processing apparatus allows a signal to pass through a transmission circuit in a positive time sequence and ,then, allows the signal to be transmitted through another transmission circuit having the same transmission characteristic in a reverse time sequence with respect to the positive time sequence. The purpose of this signal processing is to eliminate unwanted waveform distortion in a reproduced signal. While the transmission circuit is arranged to have a zero-phase characteristic, each segment of a continuous signal is processed throughout a period which is equal to at least two times a duration of an impulse response duration of the transmission circuit. In short, the Ochi et al. patent is directed to entirely an entirely different system and targets an entirely different scenario, i.e., Ochi et al. has nothing to do with the claims in the present application and it works entirely differently. For example, the very first lines of the Ochi et al. Summary (col. 2, lines 27–33) specifically state that their approach is intended to help reduce "unwanted waveform distortion" using a "frequency characteristic changing process" which is limited to a "small-size circuit", i.e., digital signal processing techniques. Importantly, the Ochi et al. approach relies upon signal processing chains which operate simultaneously on the same data using phase techniques to help detect and eliminate unwanted waveform errors. In short, the Ochi et al. approach demands simultaneous operation of the processing chains, which implies hardware devices with significant processing capabilities, memory and power. In contrast, claimed apparatus is specifically intended for resource-constrained mobile devices which have limited processing, memory and power capabilities. In this regard, the approach taken in the instant application attempts to lower the processing burden of such devices by only operating a single processing chain at any one time. Moreover, the Ochi et al. approach implies *a priori* determination and integrated hardware-based support of processing chain components relevant to a very specific set of waveform error conditions.

The instant invention involves the dynamic assembly and instantiation of processing components such as codecs, filters, packetizers, etc., in a parallel processing unit, and targets an entirely different domain, i.e., adaptation to the often changing data load and the dynamic transmission characteristics of IP networks, such as the Internet. Furthermore, the approach in the instant application specifically claims real-time operation with zero delay. In contrast, the Ochi et al. approach is specifically <u>not</u> intended for real-time, low-delay scenarios and relies upon parallel processing components which are characterized by significant delay and intended for broadcast scenarios.

As shown in Figure 1 of Ochi et al., an input terminal 10 and a first transmission circuit 11 having a transmission characteristic G are provided. Also, a first memory circuit 12 having a storage capacity of M which is equivalent to at least more than two times the impulse response duration α of the transmission circuit 11, is provided for storing an input signal in a predetermined time sequence and transmitting the same in the reverse of the time sequence for the length M of time. A second memory circuit 13 having a storage capacity of M which is equivalent to at least more than two times the impulse response duration α of the transmission circuit 11, is arranged for storing an input signal in a given time sequence and transmitting the same in the reverse of the time sequence for the period M after a delay time ranging from α to M-α from the action of the first memory circuit 12. Elements 14 and 15 are second and third transmission circuits which have the same transmission characteristic as that of the first transmission circuit 11. A third memory circuit 16 and a fourth memory circuit 17, each having an equal storage capacity M, are arranged for storage of an input signal in a given time sequence and transmission of the same in the reverse of the time sequence for the period M. A switch circuit 18 is also provided for transmitting during the period M an output signal of the third memory circuit 16 from the start of an action of the first memory circuit 12 to the start of an action of the second memory circuit 13 and an output signal of the fourth

memory circuit 17 from the start of the action of the second memory circuit 13 to the start of a succeeding action of the first memory circuit 12. A timing generator circuit 20 is provided for actuating the two memory circuits 12 and 16 and the switch circuit 18 at predetermined intervals of time. Also, a delay circuit 19 is provided for delaying an output signal of the timing generator circuit 20 and supplying to the two memory circuits 13 and 17 a resultant delay signal delayed by a given time from the start of the action of the first memory circuit 12. Element 21 is an output terminal.

In operation, an input signal (e.g., an analog or digital video signal) is fed through the input terminal 10 to the first transmission circuit 11 of transmission rate G. It is assumed that the input terminal 10 receives an input signal shown in Figure 2(a), which is expressed as a series of data blocks D1F, D1S, D2F, D2S, and so on. The signal from the first transmission circuit 11 is fed to the first memory circuit 12 where it is time base inverted at each duration (equal to the period M) from t0 to t_1, t_2 to t_4, or t_4 to t_6. The signal is then transferred to the second transmission circuit 14 where its particular data blocks including D1F, D2F, and D3F, which are spaced by more than the period α (of impulse response duration) from the switching point for time base inversion, can successfully be processed regardless of the effects of a switching action, as shown in Figure 2(b). The signal is then time base inverted by the third memory circuit 16 to a row of the data blocks shown in Figure 2(c). The second memory circuit 13 starts to operate (at a time t1) later than the first memory circuit 12. The data blocks including D1S, D2S, ad D3S shown in FIG. 2(e) are processed by the third transmission circuit 15. The switch circuit 18 selects the output of the memory circuit 16 during the periods of t_0 to t_1, t_2 to t_3, and t_4 to t_5 and of the memory circuit 17 during the periods of t_1 to t_2, t_3 to t_4, and t_5 to t_6. Accordingly, a row of the processed data blocks shown in Figure 2(h) will be released.

Figures 3(a)–3(j) illustrate the foregoing procedure using waveforms of the signal, in which Figure 3(a) is the waveform of the original input signal; Figure 3(b) is the waveform produced by the first transmission circuit 11; Figure 3(c) is the

waveform after time base inversion at unit periods of t_0 to t_2, t_2 to t_4, t_4 to t6, and so on; Figure 3(d) is the waveform after one more time base inversion action; Figure 3(f) is the waveform after time base inversion at unit periods of t_1 to t_3, t_3 to t_5, t_5 to t_7, and so on; Figure 3(g) is the waveform produced by the transmission circuit 15; Figure 3(h) is the waveform after a further time base inversion action; Figure 3(i) is the waveform of a control signal of the switch circuit 18, and Figure 3(j) is the waveform of the signal after switching action of the switch circuit 18. As apparent from Figures 3(a)–3(j), the waveform of Figure 3(j) contains emphasis characteristics including preshoot and overshoot peaks. Both the preshoot and overshoot peaks in the emphasis stay between the two clip levels S_1 and S_2 and thus, no waveform distortion will occur in the FM demodulated playback signal. The same effect will be obtained with the first transmission circuit 11 being coupled to the output of the switch circuit 18.

From the foregoing discussion, it will be apparent that Ochi et al. provide an entirely different signal processing apparatus for an entirely different purpose from that disclosed and claimed. The Ochi et al. apparatus does <u>not</u> suggest the disclosed and claimed invention.

As demonstrated above, the Sastry et al. load sharing scheme is not the same as the claimed setup of a parallel processor with subcomponents adapted for the changed data rate or network conditions. Moreover, the combination of Ochi et al. and Sastry et al. would not result in a workable system, much less the Applicants' invention. On the one hand, Ochi et al. is directed to a signal processing apparatus for a magnetic video tape recorder which allows a signal to pass through a transmission circuit in a positive time sequence and, then, allows the signal to be transmitted through another transmission circuit having the <u>same transmission characteristic</u> in a reverse time sequence with respect to the positive time sequence in order to eliminate unwanted waveform distortion in a reproduced signal, and on the other hand, Sastry et al. discloses a voice processing allocation scheme in an IP network to which multiple clients are connected via servers. Neither are related to the other, and it is unclear how

load sharing among multiple identical DSPs which support a number of simultaneous active voice calls can be used in a mechanism for eliminating unwanted waveform distortion in a magnetic video tape recorder.

Summary

In the claimed invention, Applicants achieve seamless handovers between potentially many different (arbitrary complex) processing units as a mechanism for optimizing transmission quality in packet-based networks and low-power devices (e.g.., mobile telephones). The central idea is to allow adaption between various independent instantiations of processing units, as determined by a particular operating environment. Processing units may contain arbitrary complex subcomponents (codecs, filters, packetizers, etc.) and may be available locally within a device or downloaded by standard means over a network connection. Applicants claimed invention is novel in that it supports seamless adaption between the current operating processing chain and newly instantiated chains either by feeding data simultaneously to both chains or utilizing additional processing resources for encoding within the second chain during setup.

In the claimed invention, Applicants switch the input of two or more independent processing units, where it is always guaranteed that only one of them is processing at any given time. In addition, Applicants coordinate the control sequence of parallel processing unit operations (setup, teardown or resource sharing) in order to minimize processing power requirements and allow the installation of potentially useful processing units specific to a given operational environment.

The Supreme Court in *KSR International Co. v. Teleflex Inc.* (KSR), 550 U.S. 398, 82 USPQ2d 1385 (2007) reaffirmed the familiar framework for determining obviousness as set forth in *Graham v. John Deere Co.* (Graham), 383 U.S. 1, 148 USPQ 459 (1966). As reiterated by the Supreme Court in *KSR*, the framework for the objective analysis for determining obviousness under 35 U.S.C. 103 is stated in

Graham. Obviousness is a question of law based on underlying factual inquiries. The factual inquiries enunciated by the Court in *Graham* are as follows:

1. ascertaining the scope and content of the prior art;
2. ascertaining the differences between the claimed invention and the prior art; and
3. resolving the level of ordinary skill in the pertinent art.

These principles were not changed by the Court's decision in *KSR*; rather, these principles have been reaffirmed by the Court.

ARGUMENT VIIE. REJECTION OTHER THAN 35 U.S.C. §§102, 103 AND 112

There are no other rejections other than the rejections under 35 U.S.C. §103.

VIII. CLAIMS APPENDIX

The text of the claims involved in the appeal are:

1. An apparatus for the transmission of time-synchronous multi-media data from a sender to a receiver using a IP (Internet Protocol) network, wherein the time-synchronous data is processed and transmitted at the sender as well as the receiver, comprising:

the sender receiving time-synchronous multi-media data;

a mechanism connected to said sender for processing the time-synchronous multi-media data for output to said IP network; and

the receiver connected to said IP network for receiving processed time-synchronous multi-media data transmitted over said IP network;

said mechanism comprising:

a first processing unit composed of multiple subcomponents, each subcomponent being designed to process the time-synchronous multi-media data in a specific and different way, a plurality of said multiple subcomponents of said first processng unit being selected from the group consisting of a codec, a filter and an IP packetizer;

a second processing unit parallel to the first processing unit, said second processing unit being composed of multiple subcomponents, each subcomponent being designed to process the time-synchronous multimedia data in a specific and different way, a plurality of said multiple subcomponents of said second processing unit being selected from the group consisting of a codec, a filter and an IP packetizer, wherein the subcomponents of the second processing unit are setup and adapted based on changed sender data rate or network characteristics by configuring attribute parameters of the subcomponents, wherein data processing and transmission

of the time-synchronous mulit-media data is continued within the first processing unit during the setup and adaptation of the second processing unit; and

a switch selecting between the first and second processing units, the processing and transmission of the time-synchronous multi-media data initially being performed by the first processing unit and, after switching by the switch, the processing and transmission of the time-synchronous multi-media data is performed using the second processing unit such that the processing and transmission of the time-synchronous multi-media data is performed within the second processing unit, the output of said switch being connected to said IP network.

2. The apparatus according to claim 1, wherein the setup and adaptation of the second processing is started using a trigger event.

3. The apparatus according to claim 1, wherein the switching is performed after completion of the setup and adaptation of the second processing unit.

4. The apparatus according to claim 1, wherein the switching is performed after reaching a certain switching condition.

5. The apparatus according to claim 4, wherein the certain switching condition is whether at least one given parameter reaches at a predetermined value.

6. The apparatus according to claim 1, wherein the time-synchronous multi-media data is processed in the first processing unit using a plurality of said multiple subcomponents.

7. The apparatus according to claim 6, wherein the subcomponents include at least one of a codec, a filter, a packetizer, and a memory buffer.

8. The apparatus according to claim 1, wherein the time-synchronous multi-media data is processed in the second processing unit using a plurality of said multiple subcomponents.

9. The apparatus according to claim 8, wherein the subcomponents include at least one of a codec, a filter, a packetizer, and a memory buffer.

10. The apparatus according to claim 8, wherein the subcomponents are connected during setup.

11. The apparatus according to claim 1, wherein the first and second processing unit is initialized after setup.

12. The apparatus according to claim 8, wherein each of the subcomponents of the second processing unit is adapted to the other subcomponents or changed sender data rate or changed network characteristics.

13. The apparatus according to claim 6, wherein, after switching by the switch, the subcomponents of the first processing unit are de-attached from each other.

14. The apparatus according to claim 13, wherein a plurality of the second processing units is setup and, after switching by the switch, the subcomponents of the first processing unit are included in one of the second processing units.

15. The apparatus according to claim 6, wherein after switching by the switch, the subcomponents of the first processing unit remain connected.

16. The apparatus according to claim 1, wherein a plurality of second processing units are setup and adapted based on changed data rate and network characteristics.

17. The apparatus according to claim 1, wherein an additional processing unit for the processing and transmission of time-synchronous multi-media data is used in sequence with the first and second processing units.

18. The apparatus according to claim 1, wherein the time-synchronous multi-media data is gathered with one of mechanisms for acquiring visual data and speech data.

IX. EVIDENCE APPENDIX

1. Declaration of Koichi Funaya under 37 C.F.R. §1.132
2. Harry Newton, *Newton's Telecom Dictionary*, pages 341, 465, and 537
3. Wikipedia entries for "High-definition television", "Non-linear editing system", and "Video processing expansion card"
4. ATI White Paper entitled "Video 101"
5. matrox RT.X2 Release 3.1, "Professional realtime HD and SD editing platforms"
6. Turtle Beach, "Video Advantage PCI"

X. RELATED PROCEEDINGS APPENDIX

There are no related proceedings regarding this application.

Conclusion and Request for Reversal

It is respectfully submitted that the claims have been misinterpreted by the Examiner in his rejections under 35 U.S.C. §103. Moreover, the Examiner has misinterpreted the references he relies on to reject the claims. The fact is that the most relevant prior art is that which Applicants have disclosed in Figures 1 and 2 of their application. That prior art has the problem of dropping frames in the transmission of time-synchronous multimedia data over an IP network, such as the Internet, under conditions of changing data load and network characteristics. The claimed invention solves that problem by setting up a parallel processing unit which is adapted to changed data load and/or network characteristics and seamless switching to the parallel processing unit.

Reversal of the Examiner's rejections under 35 U.S.C. §103 and issuance of the patent is therefore respectfully requested.

Respectfully submitted,

C. Lamont Whitham
Reg. No. 22,424

Whitham, Curtis, Christofferson & Cook, P.C.
11491 Sunset Hills Road, Suite 340
Reston, VA 20190
Tel. (703) 787-9400
Fax. (703) 787-7557

Customer No. 30743